

PCTWORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶: G03F 7/20	A1	(11) International Publication Number: WO 97/48021 (43) International Publication Date: 18 December 1997 (18.12.97)
(21) International Application Number: PCT/US97/09298 (22) International Filing Date: 10 June 1997 (10.06.97) (30) Priority Data: 60/019,490 10 June 1996 (10.06.96) US (71) Applicant (for all designated States except US): HOLOGRAPHIC LITHOGRAPHY SYSTEMS [US/US]; Three Preston Court, Bedford, MA 01730 (US). (72) Inventor; and (75) Inventor/Applicant (for US only): HOBBS, Douglas, S. [US/US]; 1998 Massachusetts Avenue, Lexington, MA 02173 (US). (74) Agent: EDELL, Ira, C.; Epstein, Edell & Retzer, Suite 400, 1901 Research Boulevard, Rockville, MD 20852 (US).		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published With international search report.
(54) Title: PROCESS FOR MODULATING INTERFEROMETRIC LITHOGRAPHY PATTERNS TO RECORD SELECTED DISCRETE PATTERNS IN PHOTORESIST		
(57) Abstract A double exposure process is disclosed whereby a first exposure produced by conventional photolithographic techniques generates a latent negative image in a photoresist etch mask layer (22), the image subsequently employed to modulate a second exposure generated by the multiple beam interferometric lithography technique. Periodic surface relief structures (80) patterned by the second exposure and formed after development of the exposed photoresist material, are restricted to regions (52) defined by the initial exposure, with the photoresist material (54) outside these regions remaining unmodulated, or devoid of the periodic structures (80), and suitable for use as a mask in a subsequent etching process.		

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakhstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

Process for Modulating Interferometric Lithography
Patterns to Record Selected Discrete Patterns in Photoresist

BACKGROUND OF THE INVENTION

This is a continuation of U.S. provisional application serial number 60/019,490, filed June 10, 1996.

Field of the Invention:

The present invention relates to a process for producing a plurality of discrete arrays of sub-micron structures in a photoresist etch mask by interferometric or holographic lithography techniques; each of the arrays is bounded by regions not subjected to the interferometric lithography.

Discussion of the Prior Art:

Holographic or interferometric lithography is now a proven technology for creating structures having sizes smaller than a micron in a continuous, two-dimensional, periodic array. For example, U. S. Patents 4,402,571, and 4,496,216, to Cowan, et al. and 5,142,385, to Anderson et al., the entire disclosures of which are incorporated herein by reference, disclose methods and apparatus for producing a periodic and continuous surface relief pattern in a surface by exposing a photosensitive material to a laser

interference fringe pattern and then developing the photosensitive material. Interferometric lithography exploits the mutual coherence of multiple optical beams derived from a single laser; the beams are overlapped in a selected region of space and interfere to produce patterns of light and dark areas, or fringe patterns, repeating on a scale proportional to the laser wavelength. The fringe patterns are recorded in photosensitive media such as photoresist. Conventional contact or projection photomasks are not required and so interferometric lithography has become known as "maskless" lithography.

Interferometric lithography has been used in a laboratory environment in attempting to produce a flat panel display having a distributed cathode; the display is known as a Field Emission Display (FED). A FED is a distributed cathode, flat panel analog to the well known Cathode Ray Tube (CRT) and can include billions of microscopic cathode electron 'guns' in an array distributed over the surface of a display substrate. Electrons emitted from the microscopic, cone shaped cathodes, under the influence of a large accelerating potential, strike a phosphor screen disposed opposite a common anode, and are thereby converted to photons (i.e., light). In making the cathode matrix in a FED, it has been discovered that the most critical fabrication step is patterning of an array of high resolution features such as holes or cathode emitter tips. In the prior art, a photosensitive medium such as photoresist was employed to record an image of a hole array formed by a conventional photolithographic technique such as contact printing with shadow masking techniques, optical projection, or electron beam writing. The array of holes in photoresist was then used as an etch mask in forming the emitter wells.

It would be desirable to use interferometric lithography in making an etch mask for fabricating FEDs, but the continuous nature of interferometric lithography fringe patterns is not suitable for use in an etch mask which must have cathode cone holes (or tips) only in preselected pixel or sub-pixel regions. In other technologies, a similar problem exists, for example, in making a Dynamic Random Access Memory (DRAM), Central Processing Unit (CPU) or a logic chip, high density patterns in an etch mask must be confined within or combined with other patterns for leadouts, contact vias or individual device area patterns. There is a need, therefore, for a method to selectively negate exposure to interferometric fringe patterns in areas outside selected regions such as the pixel region,

but without a requirement for removing the photoresist. There is also a need for a method or process for making an etch mask for producing FEDs which requires the fewest number of process steps and which can be completed in the least amount of time, to satisfy economic requirements as dictated by the marketplace.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is a primary object of the present invention to overcome the above mentioned difficulties by providing a method for making an etch mask having a plurality of discontinuous and discrete arrays containing a high density of high resolution features created by interferometric lithography.

Another object of the present invention is providing an efficient and effective method for making an etch mask segmented in a selected number of discontinuous subareas in which high resolution interferometric lithography can be used to provide sub-micron sized structures.

The aforesaid objects are achieved individually and in combination, and it is not intended that the present invention be construed as requiring two or more of the objects to be combined unless expressly required by the claims attached hereto.

In accordance with the method of the present invention, patterns of sub-micron structures in a photoresist etch mask are produced by interferometric or holographic lithography techniques after image-wise exposure using photolithographically generated pattern overlays. In the first step, negative pattern overlays are used to create a plurality of sub-pixel regions of blocked or shaded photoresist bounded by a larger, rectangular region of exposed or illuminated photoresist. In the second step, the photoresist etch mask layer is chemically affected, either thermally or by flooding or immersion in a gaseous or liquid environment, such as saturation with ammonia vapor, thereby rendering the formerly exposed rectangular region of photoresist insensitive to further light exposure and insoluble in subsequent etching steps. In the third step, a sub-micron, high resolution light interference pattern is modulated or apertured in the photoresist layer etch mask, in situ, by the now insensitive, low resolution photoresist negative pattern, whereupon the light interference pattern causes periodic arrays of sub-micron exposed spots only in sub-pixel

regions of the light sensitive photoresist. In the fourth step, the photoresist layer is chemically developed and the exposed spots are etched away, leaving a plurality of discrete (i.e., separate) periodic arrays of sub-micron holes in the etch mask.

The above and still further objects, features and advantages of the present invention will become apparent upon consideration of the following detailed description of a specific embodiment thereof, particularly when taken in conjunction with the accompanying drawings, wherein like reference numerals in the various figures are utilized to designate like components.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1a is an overhead view of a single pixel in a field emission display, illustrating method step one, an initial light exposure delineating sub-pixel regions as defined by a cathode mesh adapted to contain an array of half-micron holes to be patterned using a holographic technique in subsequent steps.

Fig. 1b is a cross-sectional view of the single pixel taken along line A-A' of Fig. 1a illustrating the initial light exposure to delineate sub-pixel regions.

Fig. 2a is an overhead view the single pixel, illustrating method step two, saturation with ammonia vapor of the photoresist bearing the latent image formed by the exposure of the step of Fig. 1a.

Fig. 2b is a cross-sectional view of the single pixel illustrating the saturation step taken along line A-A' of Fig. 2a.

Fig. 3a is an overhead view of the single pixel, illustrating method step three, a holographic or interferometric exposure to form a latent image of an array of half-micron areas of high luminous intensity.

Fig. 3b is a cross-sectional view of the single pixel illustrating the holographic exposure step taken along line A-A' of Fig. 3a and showing the placement of the half-micron areas of high luminous intensity.

Fig. 4a is an overhead view of the single pixel, illustrating the resulting photoresist etch mask layer after method step four, a development step, leaving a plurality of periodic arrays of etch mask holes disposed only in the sub-pixel regions.

Fig. 4b is a cross-sectional view of the single pixel taken along line A-A' of Fig. 4a, illustrating the resulting photoresist etch mask layer, after development.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In accordance with standard industry practice, a layer of positive photoresist material is coated onto a suitable substrate material such as glass, silicon or sapphire.

Referring specifically to Figs. 1a and 1b of the accompanying drawings, an overhead view of a subsection of a field emission display substrate 10 corresponds to the area required for a single pixel 12 including a cathode mesh 14. Fig. 1a includes an imaginary planar layer 15 of light and shaded regions illustrating incident light (or the lack thereof) in an imaginary cross section. In a first method step using conventional photolithographic techniques such as shadow masking (i.e., contact printing) or optical projection, an initial, negative pattern, image-wise exposure to light includes sixteen square blocked (i.e., shaded or dark) areas 18 all within and bounded by an illuminated, substantially rectangular mesh-shaped area 20. The pattern shown in Fig. 1 is a pixel area definition image, as is required during manufacture of a FED panel. Blocked or dark areas 18 delineate sub-pixel regions as defined by cathode mesh 14. Fig. 1b is a cross-sectional view of the single pixel 12 taken along line A-A' of Fig. 1a, and illustrates the initial light exposure to delineate blocked sub-pixel regions 18 in a 6000Å thick photoresist layer 22.

As shown in Fig. 1b, display substrate 10 includes a substantially planar glass base layer 30 having an upper surface 32 opposing a lower surface 34. A 5000Å thick Molybdenum and Silicon (Moly/Si) layer 36 is adhered to glass base layer upper surface 32 and includes sixteen square, discrete Silicon (Si) sub pixel regions 38 all within and bounded by a Molybdenum (Moly) cathode mesh 14 electrically connected to the cathode line 40 as shown in Fig. 1a. A 4000Å thick Silicon Dioxide (SiO₂) layer 42 is disposed upon and adhered to an upper surface of the Moly/Si layer 36, opposite the glass base layer 30. A 1000Å thick Niobium (Nb) gate layer 44 is disposed upon and adhered to an upper surface of the SiO₂ layer 42, opposite the Moly/Si layer 36 and is electrically connected to the gate line 45 as shown in Fig. 1a. The photoresist (PR) layer 22 is disposed upon and adhered to an upper surface of the Nb layer 44, opposite the SiO₂

layer 42, and has an uppermost surface 46, part of which is exposed to the light in region 48 (i.e., corresponding to a portion of illuminated area 20 as seen in imaginary layer 15) during the first step. The exposure to the light during the first step chemically alters the composition of the illuminated and exposed area 20 of the photoresist layer 22, as is well known in the art.

As shown in Figs. 2a and 2b, the second method step is exposure or saturation with ammonia vapor (illustrated schematically as layer 50) of the photoresist layer 22, now bearing the latent image formed by the light exposure of the first method step illustrated in Fig. 1a. The latent image includes sixteen square, unaffected and previously blocked or shaded regions 52 all within and bounded by an affected, previously illuminated, substantially rectangular area 54 corresponding to the illuminated area 20 in Figs. 1a and 1b. The unaffected regions 52 correspond to the sub-pixel regions of blocked areas 18 in Figs. 1a and 1b. In the second step, photoresist etch mask layer 22 is chemically altered or affected, either by flooding or immersion in a gaseous or liquid environment (e.g., saturation with ammonia vapor 50 heated to a temperature at or above one hundred degrees Celsius for a period of approximately ten minutes) or thermally, as is known in the art, thereby rendering the formerly exposed rectangular region 54 of photoresist insensitive to further light exposure and insoluble in subsequent developing steps. The step of chemically affecting photoresist etch mask layer 22 may be carried out in an image reversal oven, a conventional component in most semiconductor fabrication facilities. Alternatively, a chemical compound is added to photoresist layer 22 and heated, thereby causing previously exposed sections of the photoresist layer to cross link.

Turning now to Figs. 3a and 3b, illustrating method step three, a holographic or interferometric exposure is utilized to form a latent image of a periodic array of half-micron areas of high luminous intensity 62 separated by null areas of low luminous intensity 64. In the third step, a sub-micron, high resolution light interference pattern 60 is modulated or apertured in the photoresist layer etch mask 22, in situ, by the now insensitive, low resolution photoresist negative pattern 54, whereupon the light interference pattern 60 causes sub-micron exposed spots 70 only in the light sensitive photoresist in the sub-pixel regions 52. Light interference pattern 60 is a periodic and continuous laser interference

fringe pattern created from the mutual coherence of multiple optical beams derived from a single laser; the beams are overlapped in a region of space just over the uppermost surface 46 of the photoresist layer 22 and interfere to produce areas of high luminous intensity 62 and areas of low luminous intensity 64 or fringe patterns, repeating on a scale proportional to the laser wavelength. The fringe patterns are recorded in a periodic two-dimensional close-packed array of exposed spots 70 in only the still photosensitive sub-pixel regions 52 of photoresist layer 22.

In the fourth step as shown in Figs. 4a and 4b, photoresist etch mask layer 22 is chemically developed in accordance with standard industry practice in a (preferably aqueous) liquid developer and the exposed spots 70 (Fig. 3b) are dissolved away, leaving sub-micron diameter right circular cylindrical holes 80 in and through the etch mask layer 22. Each etch mask hole 80 has a first open end 82 at the uppermost surface 46 in fluid communication with a second open end 84 at the interface between the photoresist layer 22 and the Nb layer 44. After the development step, a plurality of periodic arrays of etch mask holes 80 are disposed in the separate sub-pixel regions 52. The etch mask holes are disposed only in the sub-pixel regions 52 and are not present in the surrounding affected area 54; thus the sub-pixel regions are deemed to contain discrete (i.e., spaced or separate) arrays of sub-micron etch mask holes 80.

For purposes of defining nomenclature, the method of the present invention uses the affected and insensitive area 54 to spatially modulate or to provide an aperture for use in the interferometric lithography steps to follow. The affected and insensitive area 54 remains unmodulated or unperforated by etch mask holes and permits the photoresist layer to be used as an etch mask in the subsequent etching process used in finishing the FED.

The source of illumination used to initially expose the photoresist layer 22 can be an optical image projector with an optical mask and lenses as is known in the art, or can include a shadow mask for contact printing; alternatively, a scanning electron beam, scanning laser beam or proximity printing can be used. In each alternative, the process is an image reversal process using a negative image of a selected pattern; when using a scanning electron beam or scanning laser, the pattern may be stored in software such that

pattern software in a beam controller directs writing with the scanning (electron or laser) beam. In each of the above examples the photoresist layer is exposed using actinic radiation.

The method of the present invention may be characterized in general terms as a method for producing an etch mask in a photoresist layer over a substrate (e.g., FED display substrate 10) for lithographic processing including the following steps:

- 1) controlling the locations at which a source of illumination shines upon the photoresist layer (e.g., etch mask 22) by use of a first pattern; where the first pattern defines a first selected region (e.g., a first blocked sub-pixel area 18), a second selected region (e.g., a second blocked sub-pixel area 18) and a third selected region (e.g., an illuminated area 20), where the first selected region and the second selected region are bounded by the third selected region; and exposing the photoresist layer to illumination from the source of illumination such that illumination is not transmitted for the first pattern first selected region and the second selected region and illumination is transmitted for the first pattern third selected region, whereby the photoresist layer is not exposed in a first sub-area (e.g., regions 52) corresponding to the first pattern first selected region, and is not exposed in a second sub-area corresponding to the pattern second selected region, and is exposed in a third sub-area (e.g., region 54) corresponding to the first pattern third selected region;

- 2) exposing the photoresist layer to a reactive environment (e.g., an image reversal oven containing a fluid such as ammonia vapor); reactive environment exposure alters the photoresist layer in the third sub-area to an impervious state;

- 3) exposing the photoresist layer to a periodic pattern of interferometric illumination (e.g., pattern 60, by multiple laser beam interferometry) and altering the photoresist layer in the first and second subareas with a periodic pattern of exposed spots (e.g., spots 70), while the third sub-area is substantially insensitive to and unaffected by the interferometric illumination; and

- 4) developing the photoresist layer and removing the photoresist material only in the spots exposed to the interferometric light and within the first and second subareas to make etch mask holes (e.g., holes 80).

As an aside, it should be noted that in a completed FED, an anode (not shown) is customarily disposed in close proximity to the cathode mesh 14 and includes a glass layer coated with a conductive material and a phosphor.

A number of variations are possible. For example, the thickness of photoresist layer 22 can be in the range of 1000Å to 20,000Å. Cathode mesh 39 can be any suitable conductor. Niobium Gate layer 44 can be any suitable material which will preserve the gate function. Additionally, any arbitrarily selected region can be patterned as a first, larger area (e.g., pixel area 12) and subdivided into a plurality of subareas (e.g., sub-pixel regions 18, 52).

Having described preferred embodiments of a new and improved method, it is believed that other modifications, variations and changes will be suggested to those skilled in the art in view of the teachings set forth herein. It is therefore to be understood that all such variations, modifications and changes are believed to fall within the scope of the present invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method for producing an etch mask in a photoresist layer over a substrate for lithographic processing, comprising:

positioning a first pattern between a source of illumination and the photoresist layer, said first pattern having a first selected region, a second selected region and a third selected region, said first selected region and said second selected region being bounded by said third selected region;

exposing the photoresist layer to illumination from said source of illumination, wherein illumination is not transmitted through said first pattern first selected region and said second selected region and illumination is transmitted through said first pattern third selected region;

wherein the photoresist layer is not exposed in a first sub-area corresponding to said first pattern first selected region, and is not exposed in a second sub-area corresponding to said first pattern second selected region, and is exposed in a third sub-area corresponding to said first pattern third selected region;

exposing the photoresist layer to a reactive environment, wherein said reactive environment exposure alters the photoresist layer in said third sub-area to an impervious state;

exposing the photoresist layer to a periodic pattern of interferometric illumination and altering the photoresist layer in said first and second sub-areas with a periodic pattern of exposed spots, wherein said third sub-area is impervious to said interferometric illumination;

developing the photoresist layer and removing the photoresist material only in said exposed spots within said first and second subareas.

2. The method of claim 1, wherein said reactive environment includes a fluid reactive agent.

3. The method of claim 2, wherein said reactive agent is ammonia vapor.

4. The method of claim 1, wherein said first pattern is a field emission display pixel area definition image.

5. The method of claim 1, wherein said step of positioning a first pattern between a source of illumination and the photoresist layer comprises placing a shadow mask proximate said photoresist.

6. The method of claim 1, wherein said step of positioning a first pattern between a source of illumination and the photoresist layer comprises placing a mask in an optical image projector.

7. A method for producing an etch mask in a photoresist layer over a substrate for lithographic processing, comprising:

controlling locations at which a source of illumination shines upon the photoresist layer by use of a first pattern, said first pattern defining a first selected region, a second selected region and a third selected region, said first selected region and said second selected region being bounded by said third selected region;

exposing the photoresist layer to illumination from said source of illumination, wherein illumination is not transmitted for said first pattern first selected region and said second selected region and illumination is transmitted for said first pattern third selected region;

wherein the photoresist layer is not exposed in a first sub-area corresponding to said first pattern first selected region, and is not exposed in a second sub-area corresponding to said first pattern second selected region, and is exposed in a third sub-area corresponding to said first pattern third selected region;

exposing the photoresist layer to a reactive environment, wherein said reactive environment exposure alters the photoresist layer in said third sub-area to an impervious state;

exposing the photoresist layer to a periodic pattern of interferometric illumination and altering the photoresist layer in said first and second sub-areas with a periodic pattern

of exposed spots, wherein said third sub-area is impervious to said interferometric illumination; and

developing the photoresist layer and removing the photoresist material only in said exposed spots within said first and second subareas.

8. The method of claim 7, wherein said method step of controlling locations at which a source of illumination shines upon the photoresist layer by use of a first pattern includes reading a software file to obtain machine instructions defining said first pattern; and

executing said machine instructions in a controller controlling the source of illumination.

9. The method of claim 8, wherein said method step of exposing the photoresist layer to illumination comprises writing with an electron beam.

10. The method of claim 8, wherein said method step of exposing the photoresist layer to illumination comprises writing with a laser beam.

11. The method of claim 7, wherein said reactive environment includes a fluid reactive agent.

12. The method of claim 11, wherein said reactive agent is ammonia.

13. The method of claim 7, wherein said reactive environment is at a temperature at or above 100 degrees Celsius.

14. The method of claim 7, wherein said first pattern is a field emission display pixel area definition image.

1/4

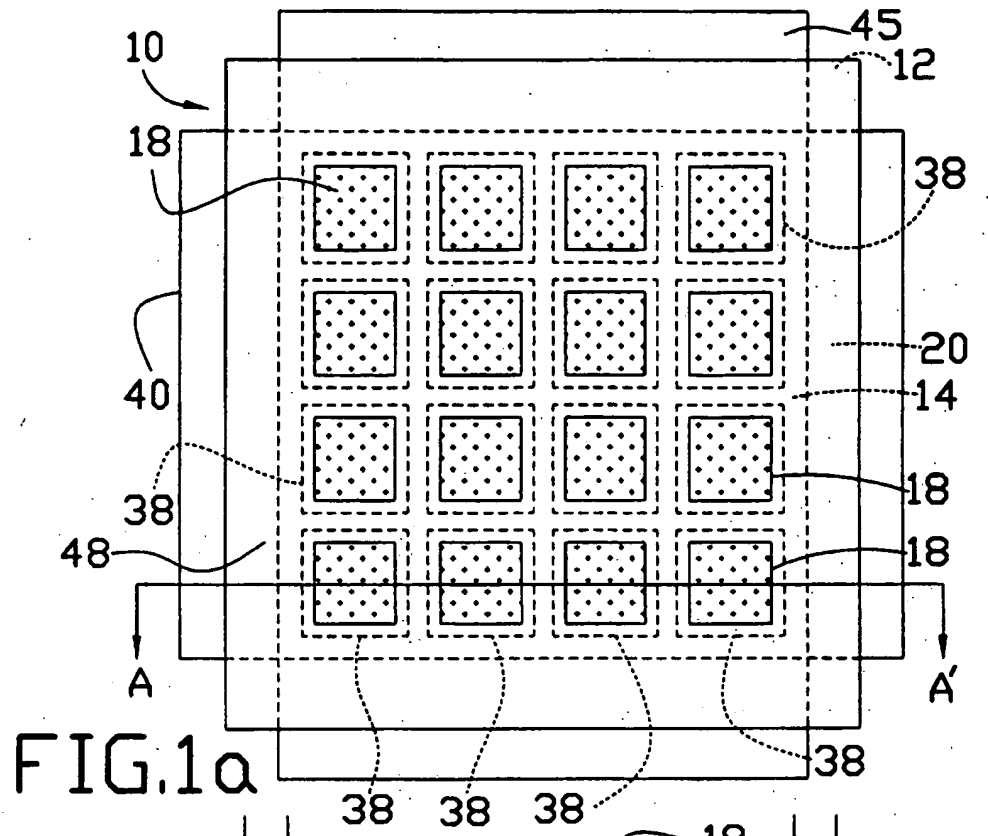


FIG. 1a

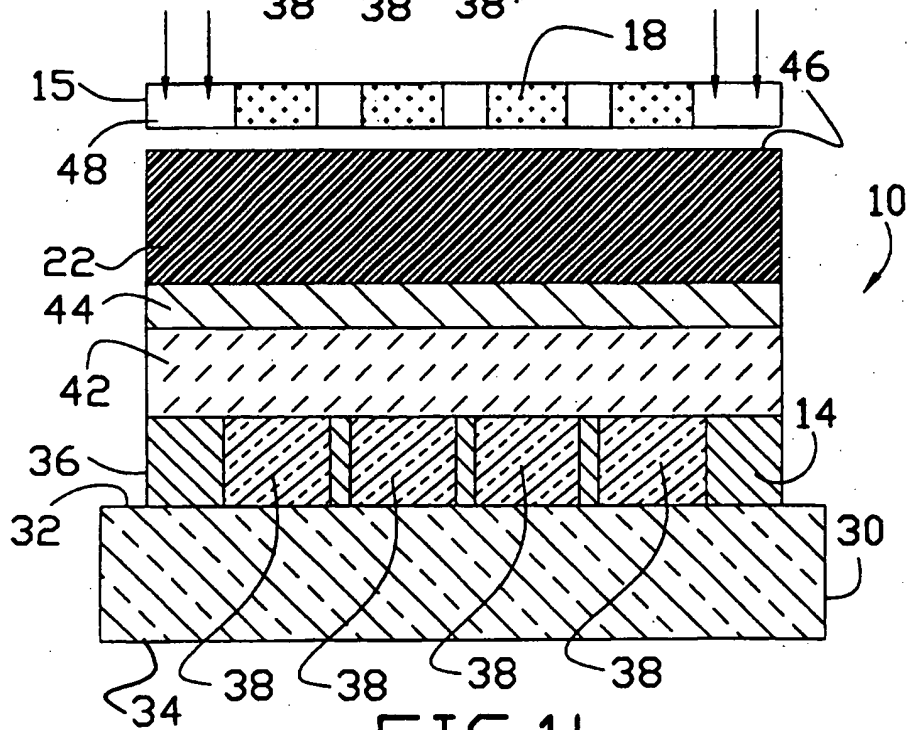
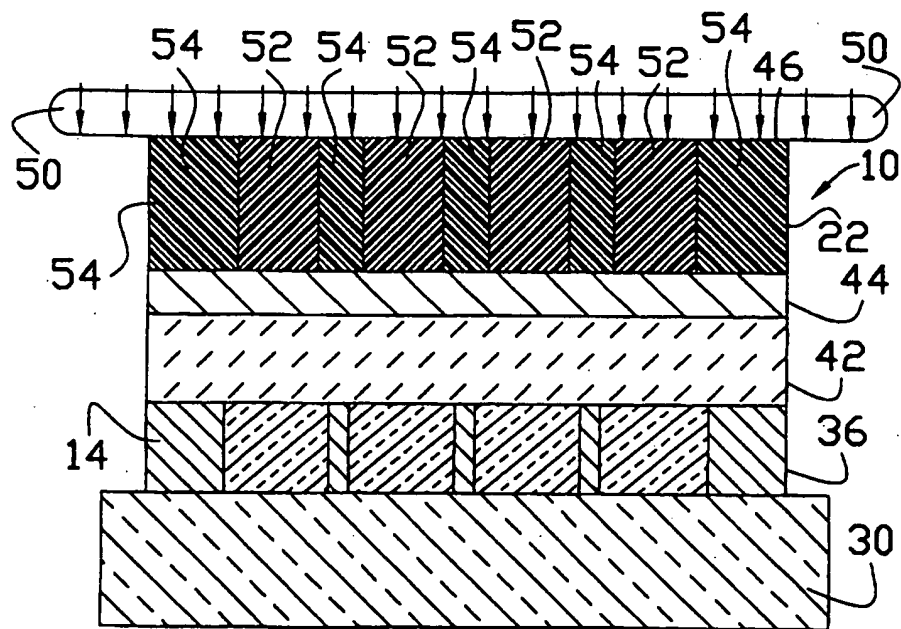
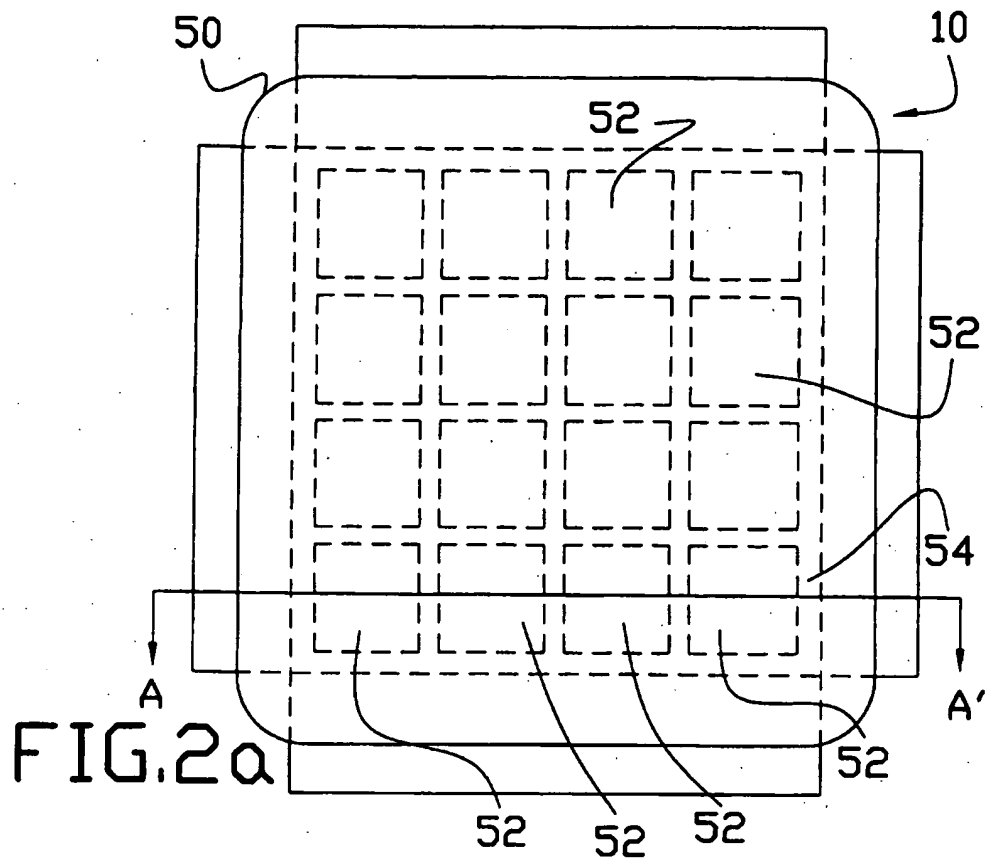


FIG. 1b

2/4



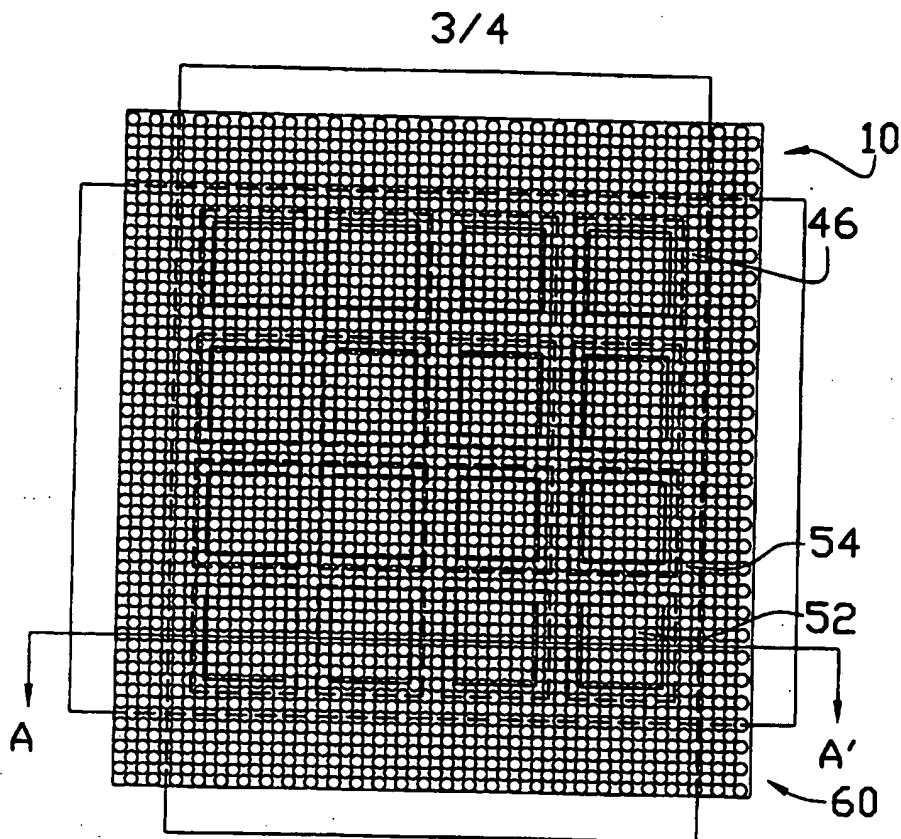


FIG. 3a

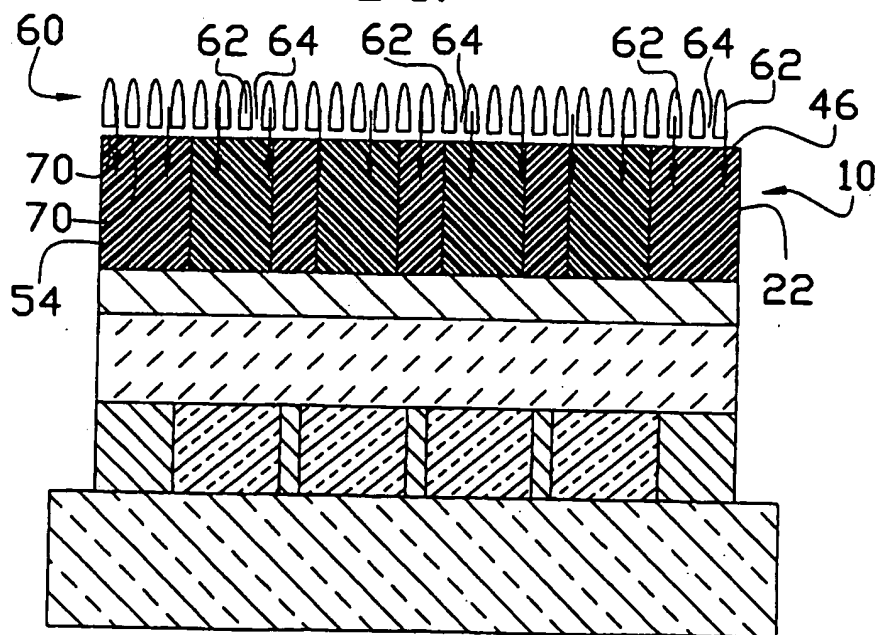


FIG. 3b

4/4

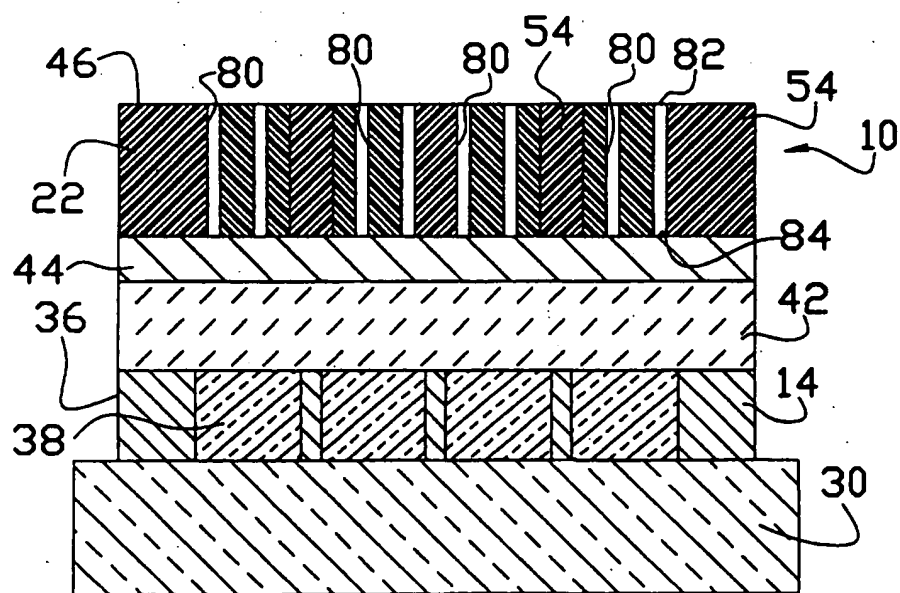
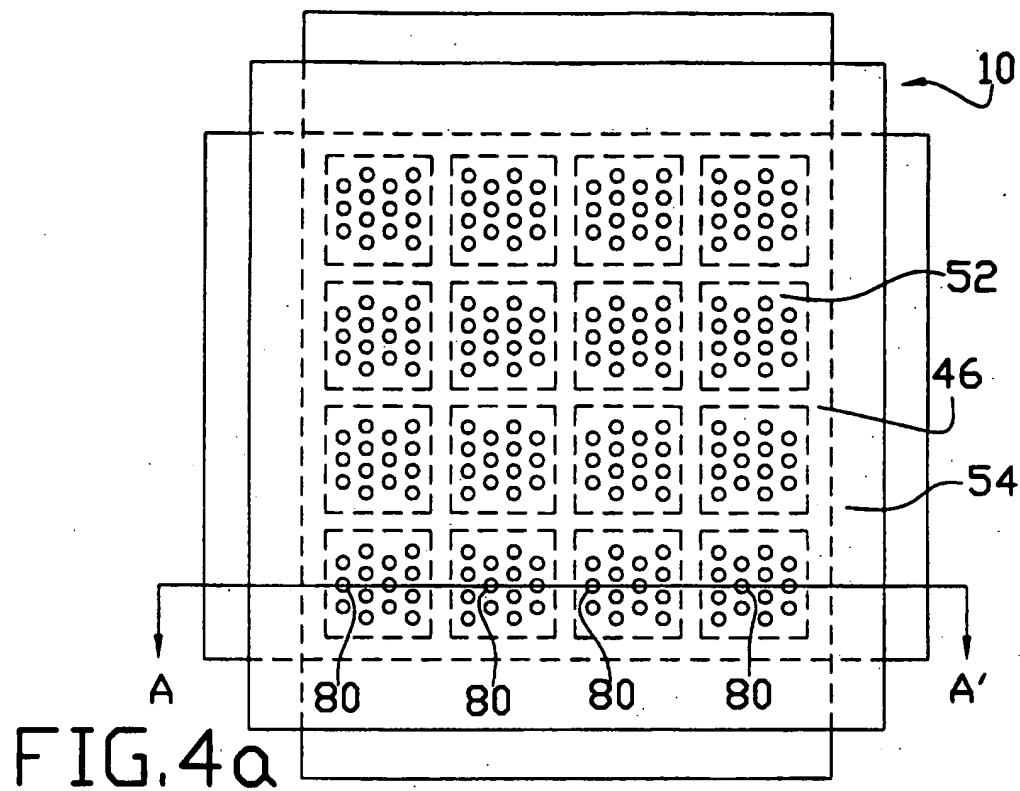


FIG. 4b

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US97/09298

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : G03F 7/20

US CL : 430/311, 5, 394, 297, 945

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 430/311, 5, 394, 296, 945

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, CAPLUS ONLINE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category ^o	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,415,835 A (BRUECK et al) 16 May 1995, col. 4, lines 53-57, table 1, col. 7, lines 12-28.	1,7 --- 2-6,8-14
Y	CHEN. X et al. Interferometric Lithography of Sub-Micrometer Sparse Hole Arrays for Field-Emission Display Applications, J. Vac. Sci. Technol., B. 1996. Vol 14. No. 5. pages 3339-3349, especially CAPLUS abstract.	4,14
Y	US 4,402,571 A (COWAN et al) 06 September 1983, col. 6, lines 12-56.	1-14

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.^o Special categories of cited documents:

A document defining the general state of the art which is not considered to be of particular relevance

E earlier document published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reasons (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T

later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principles or theory underlying the invention

X

document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y

document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other cited documents, such combination being obvious to a person skilled in the art

A

document member of the same patent family

Date of the actual completion of the international search

02 SEPTEMBER 1997

Date of mailing of the international search report

24 / 09 / 97

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

ROSEMARY ASHTON

Telephone No. 703-308-0661